Intel's 90 nm Technology: Moore's Law and More

Mark Bohr

Intel Fellow

Director of Process Architecture & Integration

Intel Research & Development

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Intel Developer Forum

Agenda

- Process Technology Evolution
- 90 nm Logic Process
- 90 nm Communication Process
- R & D Beyond 90 nm

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A New Process Every 2 Years

Process Name	P856	P858	Px60	P1262	P1264	P1266
1st Production	1997	1999	2001	2003	2005	2007
Lithography	0.25µm	0.18µm	0.13µm	90nm	65nm	45nm
Gate Length	0.20µm	0.13µm	<70nm	<50nm	<35nm	<25nm
Wafer (mm)	200	200	200/300	300	300	300

Moore's Law continues!

- Intel has been introducing new technology generations on a faster 2 year interval since 1989
- We have technologies in Intel's R&D laboratories that will drive this pace of innovation into the next decade

Logic Technology Evolution

Each new technology generation provides:

- ~ 0.7x minimum feature size scaling
- ~ 2.0x increase in transistor density
- ~ 1.5x faster transistor switching speed
- Reduced chip power
- Reduced chip cost

0.13 µm Process

Process Name	P856	P858	Px60	P1262	P1264	P1266
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Gate Length	0.20µm	0.13µm	<70nm	<50nm	<35nm	<25nm
Wafer (mm)	200	200	200/300	300	300	300

In high volume production in multiple factories for >1 year

Intel's most successful process ramp to date

Over half of Intel's microprocessors were produced on 0.13 µm in Q2 '02

90 nm Process

Process Name	P856	P858	Px60	P1262	P1264	P1266
1st Production	1997	1999	2001	2003	2005	2007
Lithography	0.25µm	0.18µm	0.13µm	90nm	65nm	45nm
Gate Length	0.20µm	0.13µm	<70nm	<50nm	<35nm	<25nm
Wafer (mm)	200	200	200/300	300	300	300

90 nm coming next!

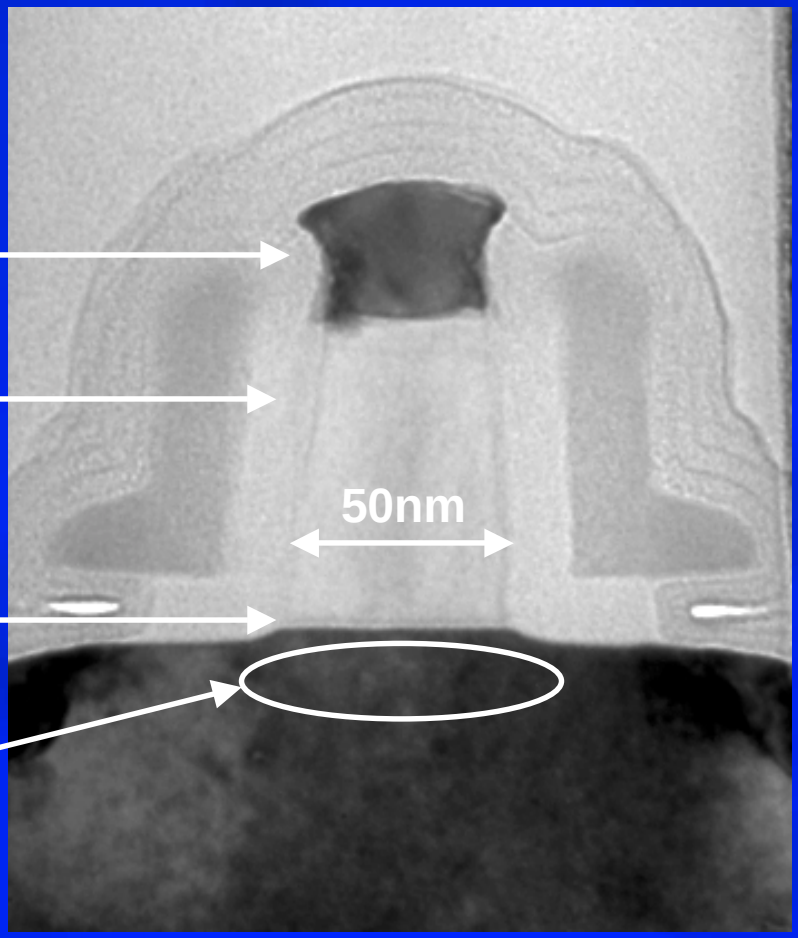
Now using nanometer (nm) instead of micron (µm)

Microns are too big! 1 µm = 1000 nm

Key 90 nm Process Features

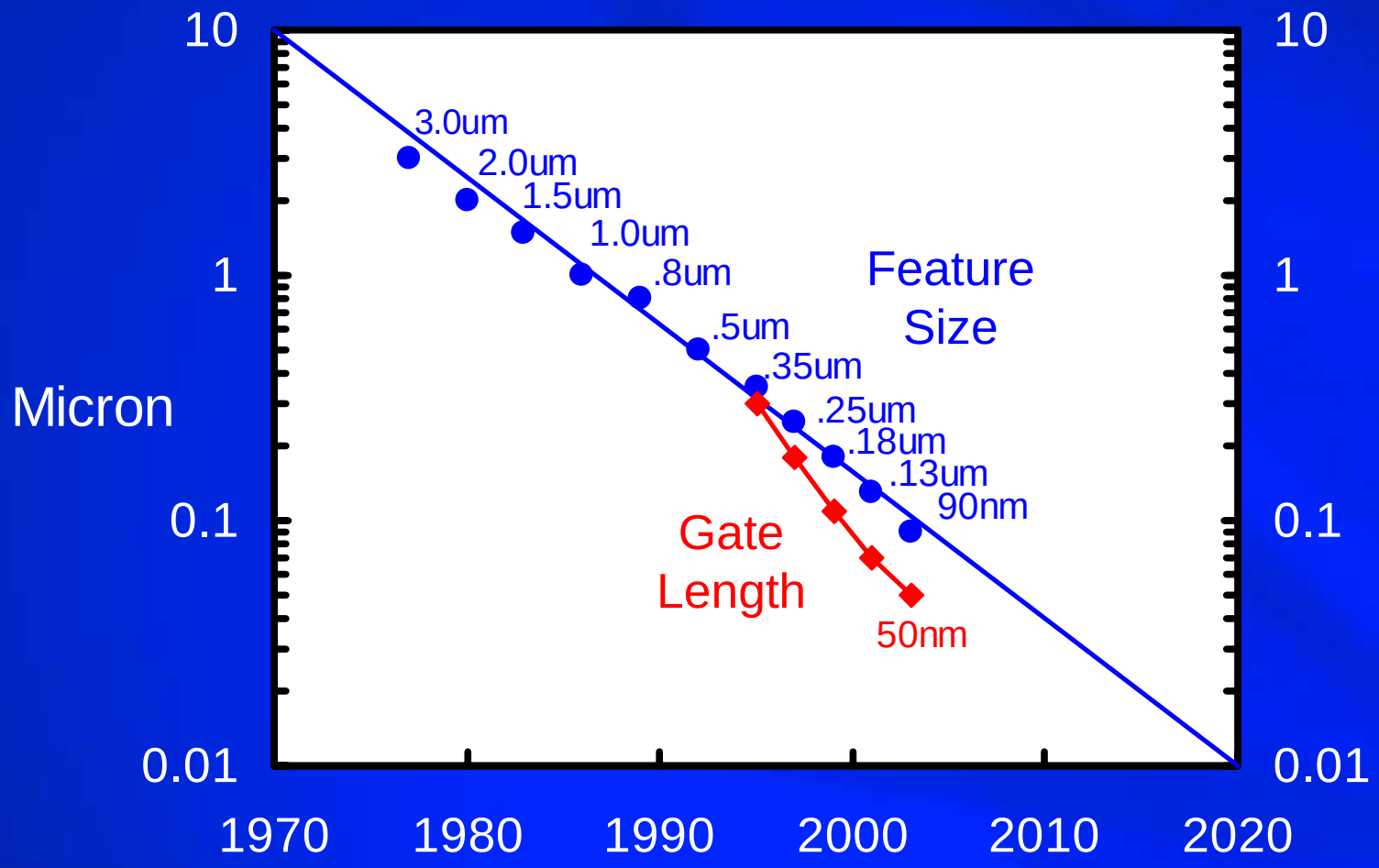
- High Speed, Low Power Transistors
  - 1.2 nm gate oxide
  - 50 nm gate length
  - Strained silicon technology
- Faster, Denser Interconnects
  - 7 copper layers
  - New low-k dielectric
- Lower Chip Cost
  - 1.0 μm^2 SRAM memory cell size
  - 300 mm wafers

90 nm Generation Transistor



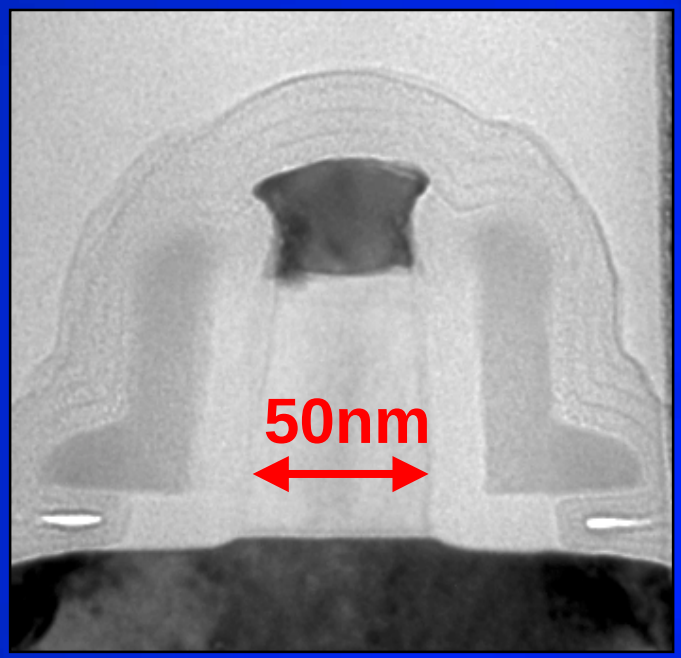
50 nm transistor dimension is ~2000x smaller than diameter of human hair

Transistor Gate Length Scaling

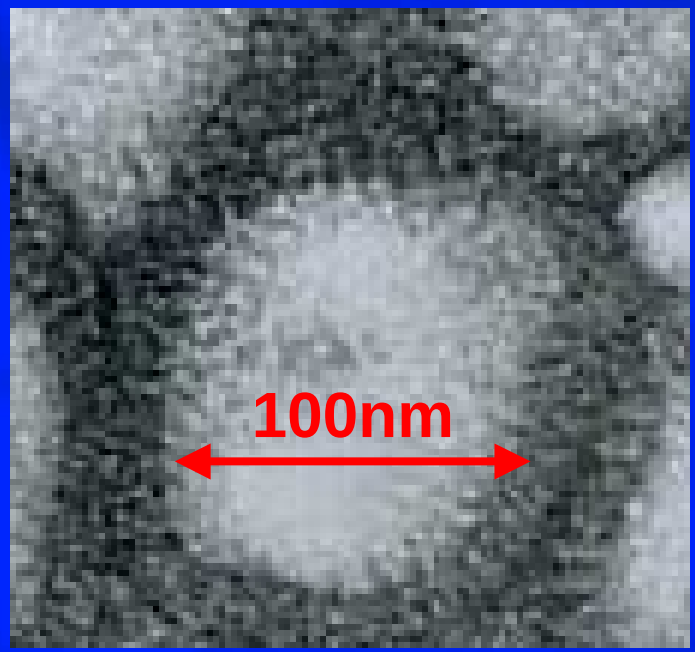


Faster gate length scaling to maintain transistor performance lead

Silicon Devices are Nanotechnology



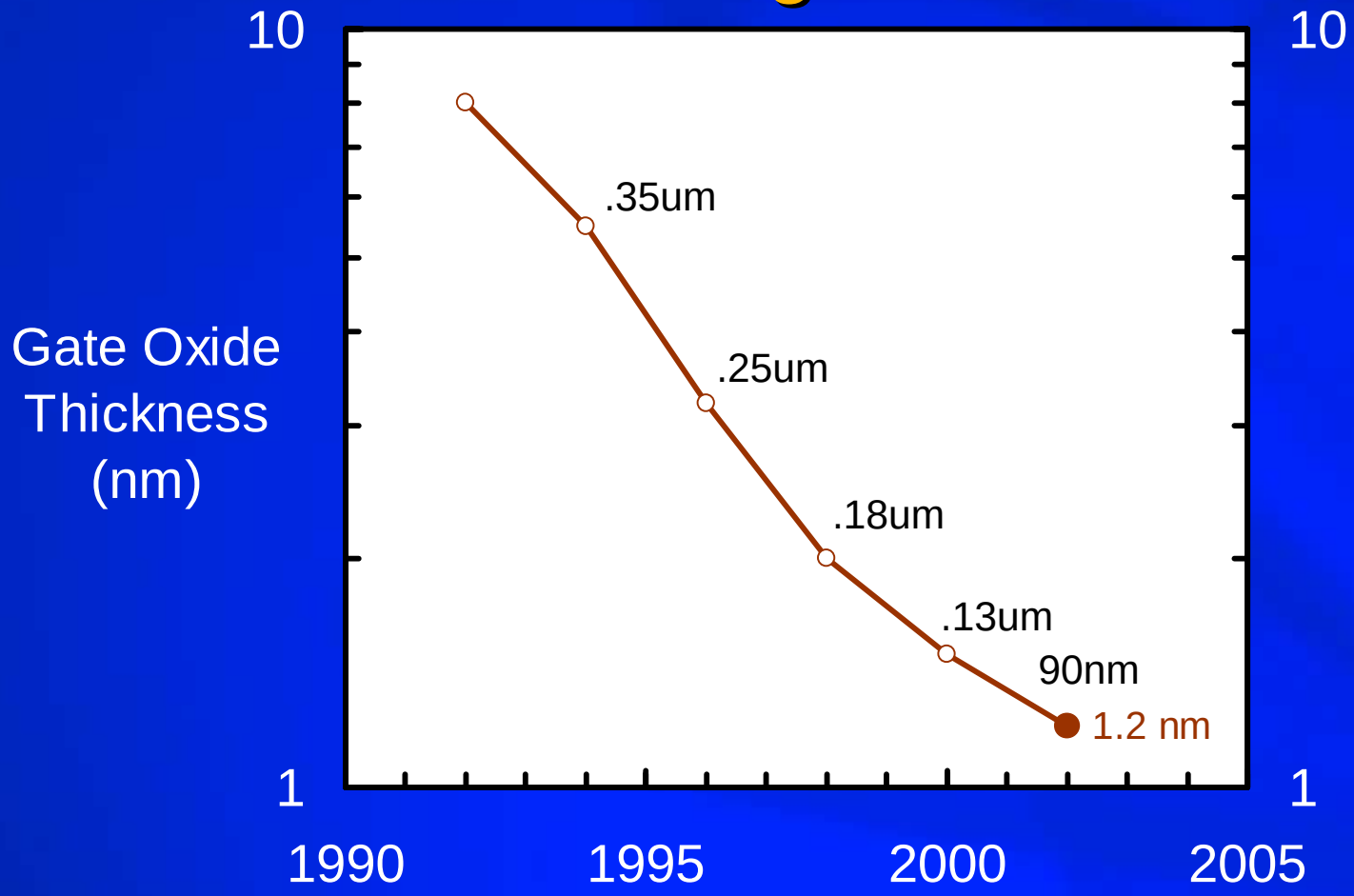
Transistor for
90 nm process



Influenza virus

Source: CDC

Gate Oxide Scaling

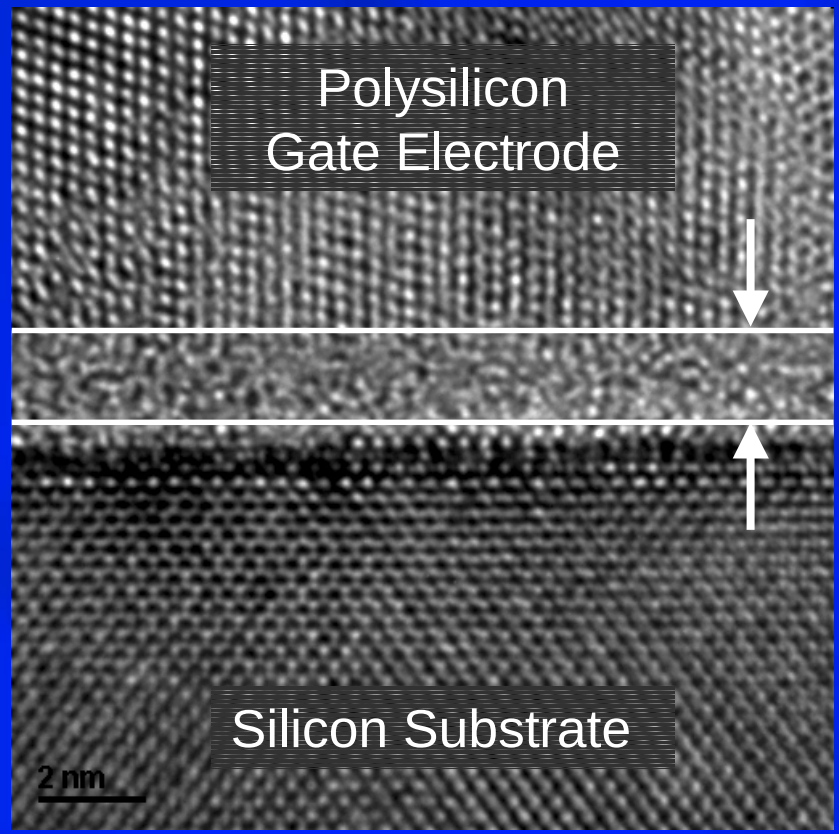


Intel leads the industry in gate oxide scaling

Thinner gate oxide increases transistor performance

90 nm Generation Gate Oxide

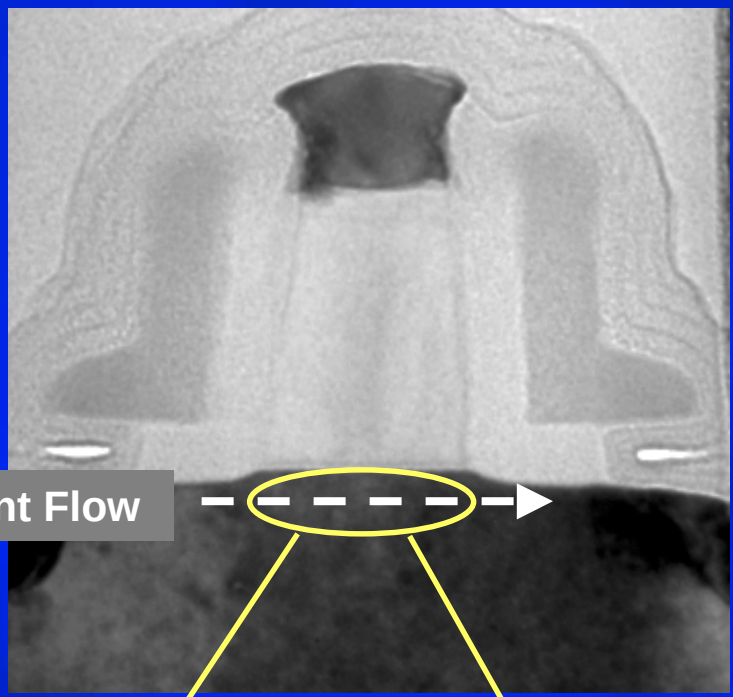
Nanotechnology is here!



1.2 nm SiO_2

Gate oxide is less than 5 atomic layers thick

Strained Silicon Transistors



Normal electron flow

Faster electron flow

Normal Silicon Lattice

Strained Silicon Lattice

Strained Silicon Transistors

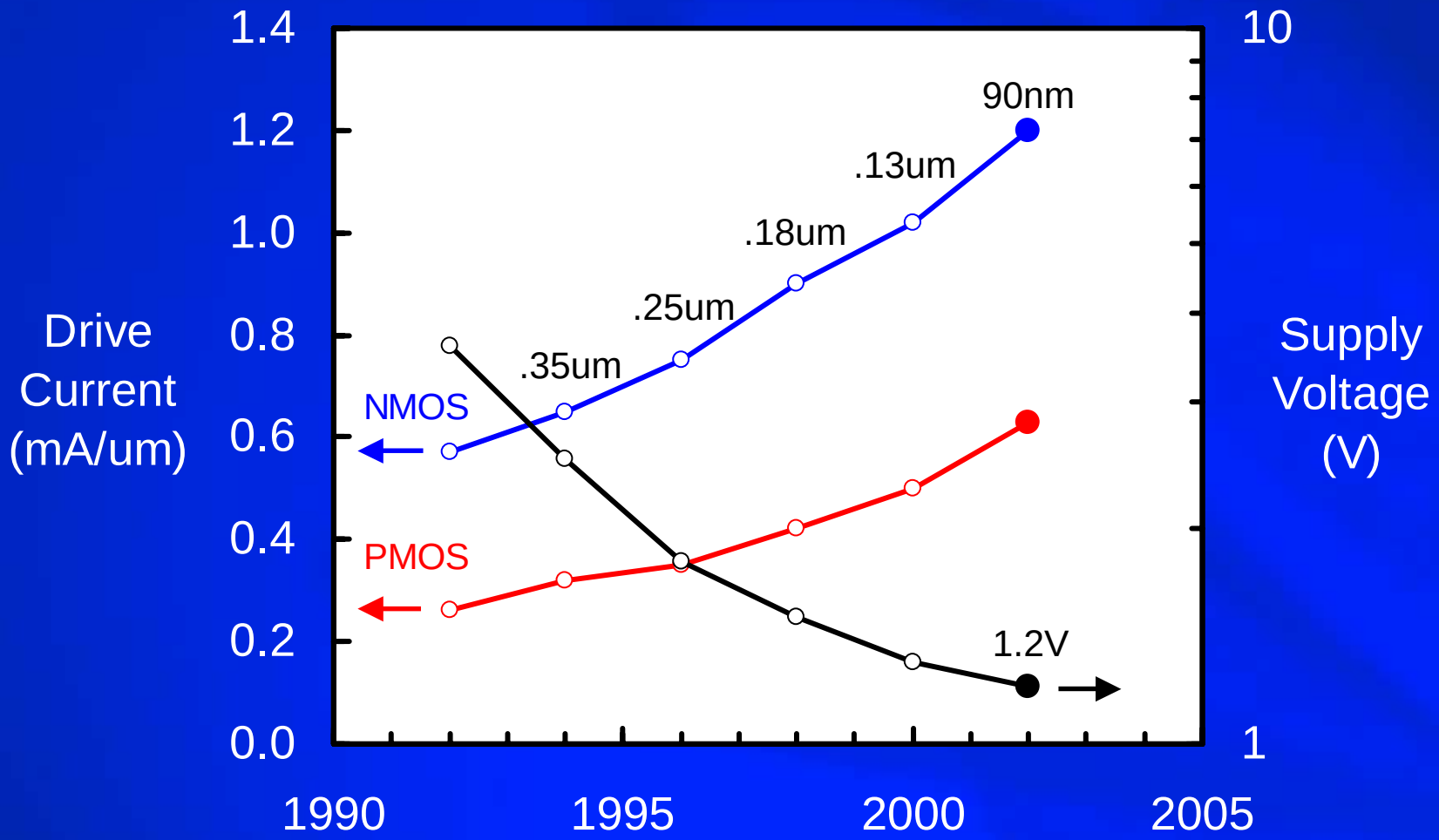
Strained silicon benefits

- Strained silicon lattice increases electron and hole mobility
- Greater mobility results in 10-20% increase in transistor drive current (higher performance)
- Both NMOS and PMOS transistors improved

Strained silicon process

- Intel's strained silicon process is unique in the industry
- No detriments to short channel behavior or junction leakage
- Added process steps increase total process cost by only ~2%

Transistor Performance



Highest drive current in the industry

Reduced supply voltage for lower power

90 nm Generation Interconnects

7 layers of copper interconnect

- 1 more layer than 0.13 μm generation
- Extra layer provides cost effective improvement in logic density

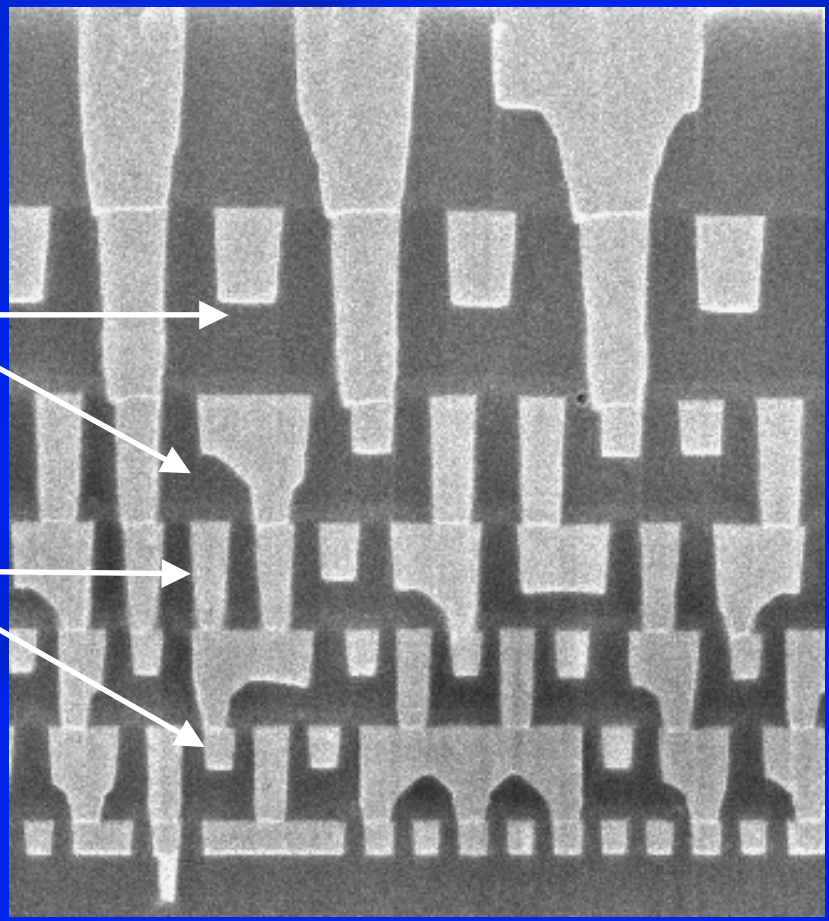
New low-k dielectric introduced to reduce wire-wire capacitance

- Carbon-doped oxide (CDO) dielectric reduces capacitance by 18% compared to SiOF dielectric used on 0.13 μm
- Reduced capacitance speeds up intra-chip communication and reduces chip power

90 nm Generation Interconnects

Low-k CDO Dielectric

Copper Interconnects

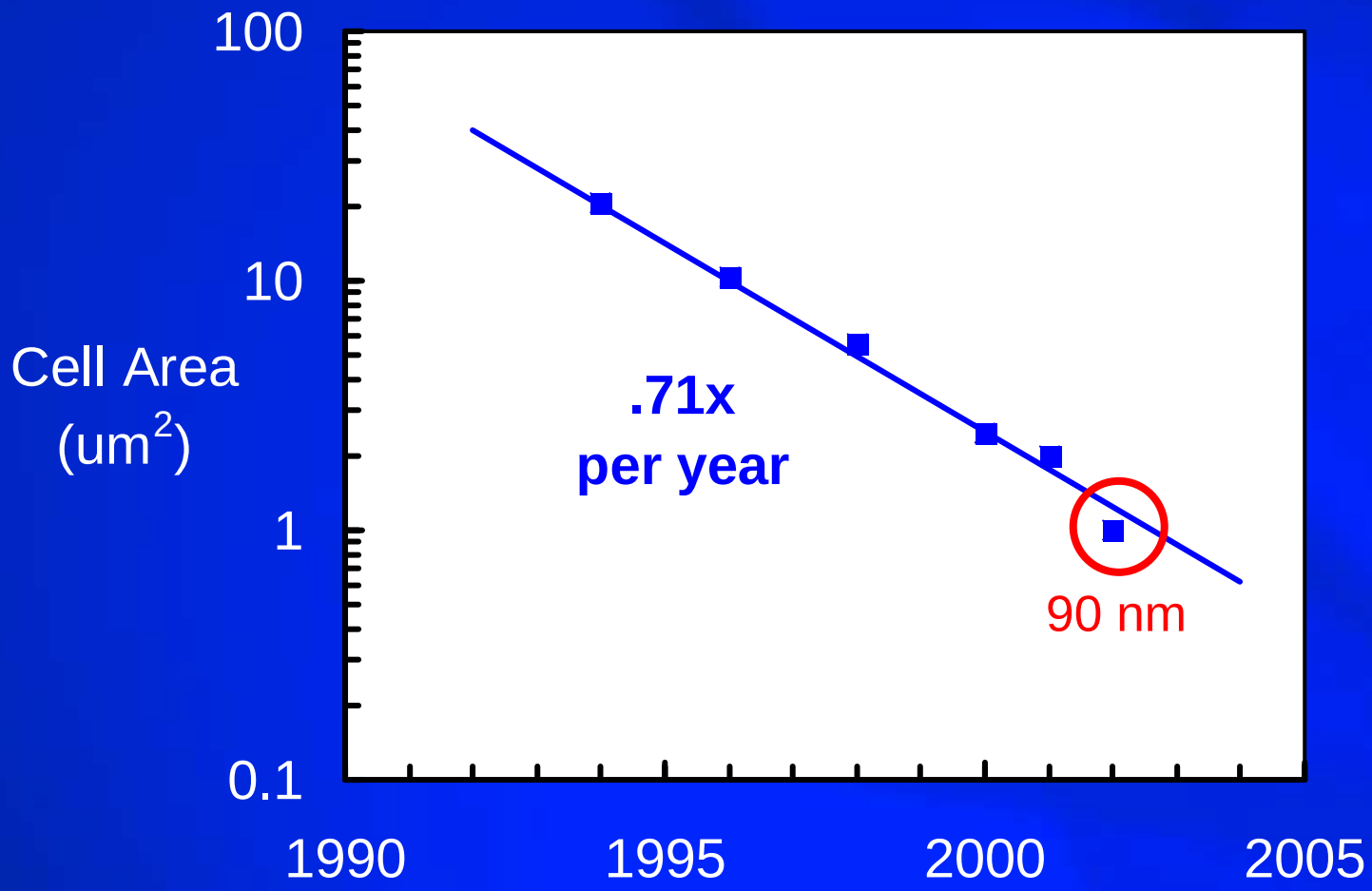


Combination of copper + low-k dielectric now meeting performance and manufacturing goals

1.0 μm^2 SRAM Cell

- Ultra-small SRAM cell used in 90 nm process packs six transistors in an area of 1.0 μm^2
- Intel was first in the industry to reach this cell size milestone
- Small memory cell enables cost effective increase in CPU performance by adding more on-die cache memory

SRAM Cell Size Trend

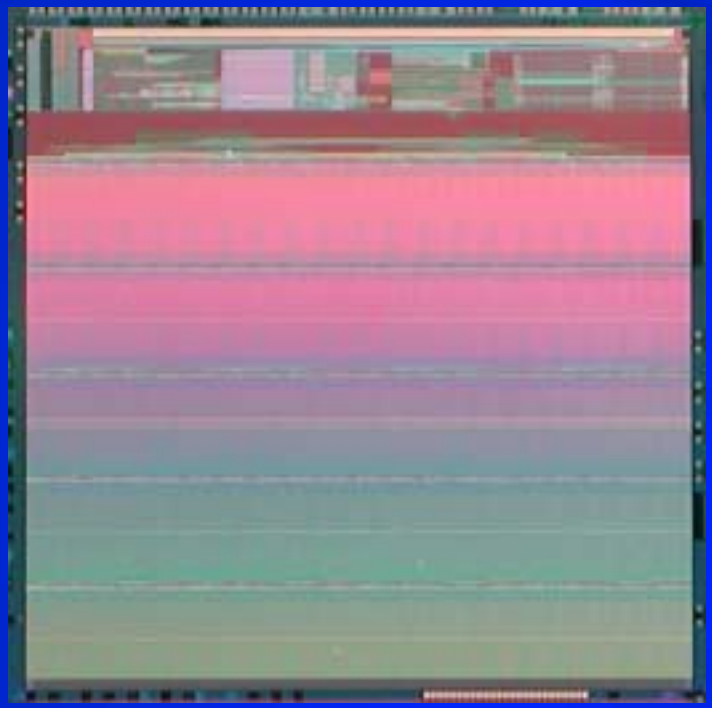


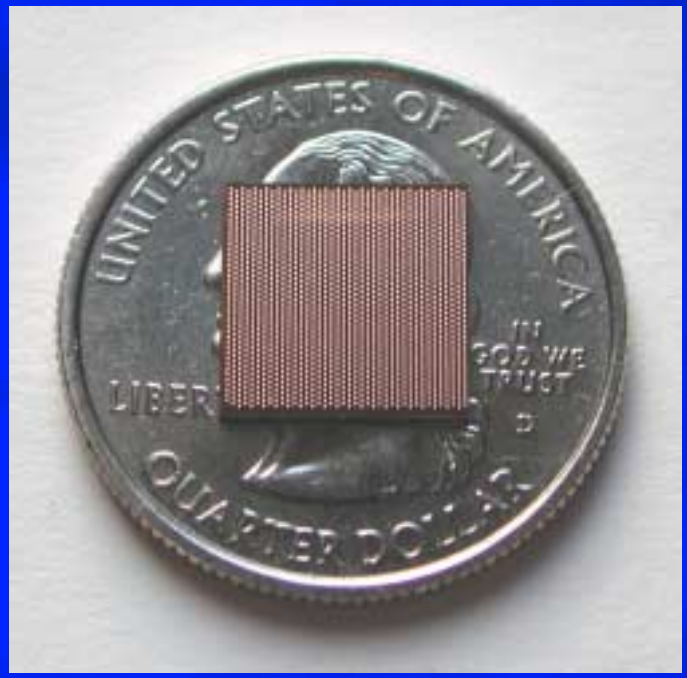
90 nm cell size is less than half
the size of 0.13 µm cell

52 Mbit SRAM on 90 nm Process

10.1 mm

10.8 mm





330 million transistors on single chip

Highest capacity SRAM in the industry

Perfect chips made with all 52 Mbits working

Same Process for Logic and SRAM

- Microprocessors use same transistors and interconnects for Logic and SRAM
- On-die SRAM cache transistor count increasing for improved performance

  0.18µm Xeon® Processor

  48M SRAM, 110M total

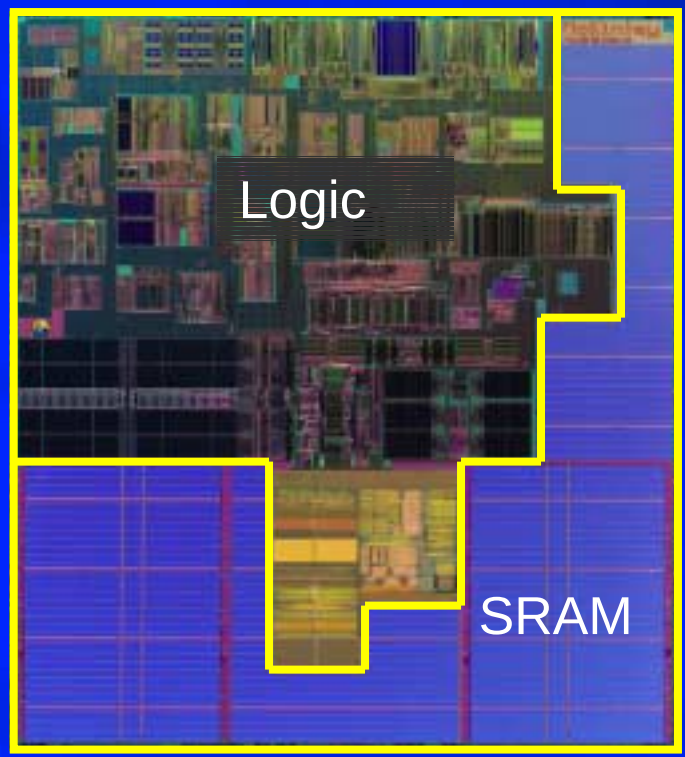
  0.18µm Itanium® 2 Processor

  144M SRAM, 220M total

  Madison (future member of Itanium processor family)

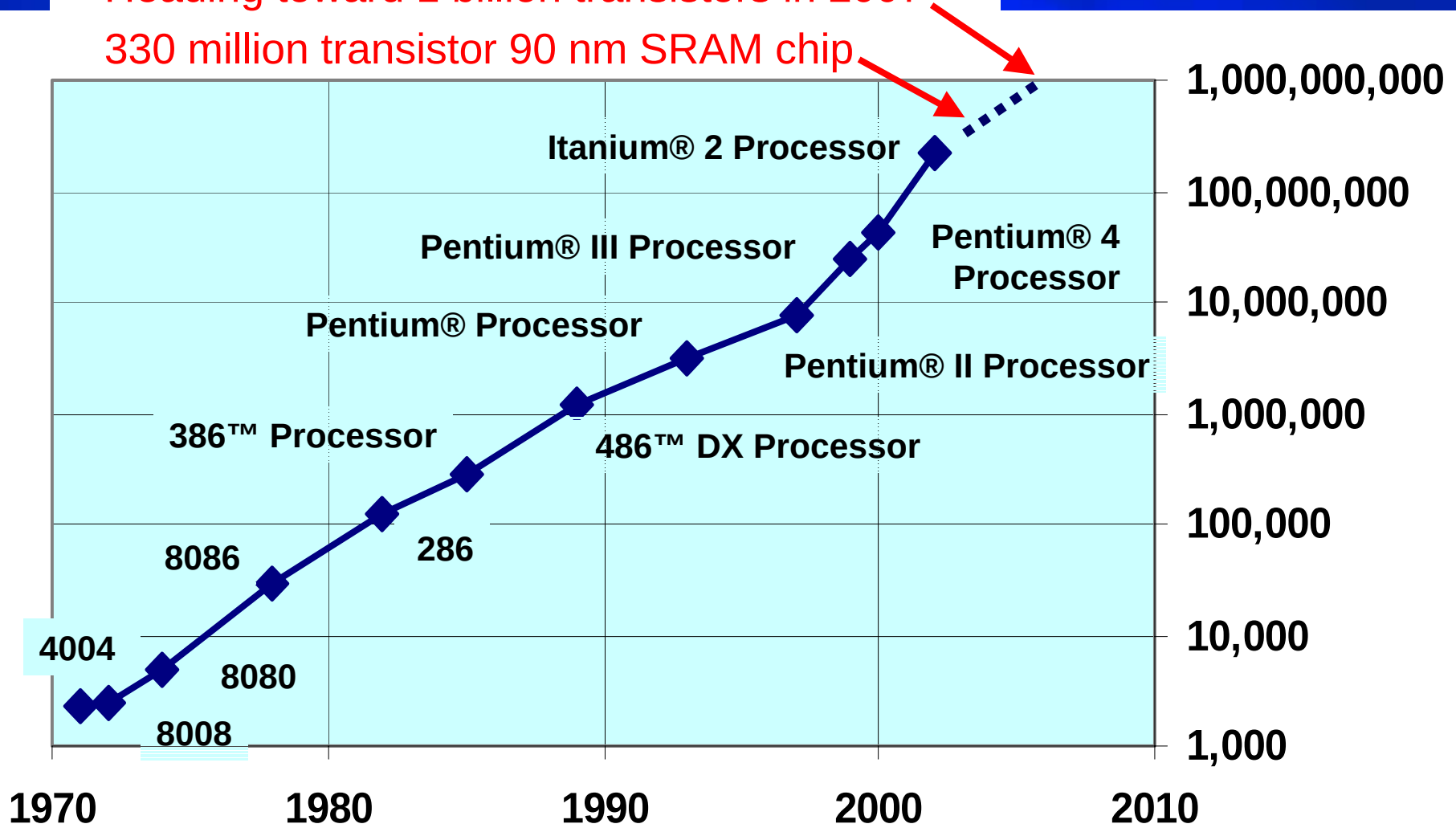
  288M SRAM, ~500M total

- 52 Mbit SRAM uses same process for 90 nm microprocessors



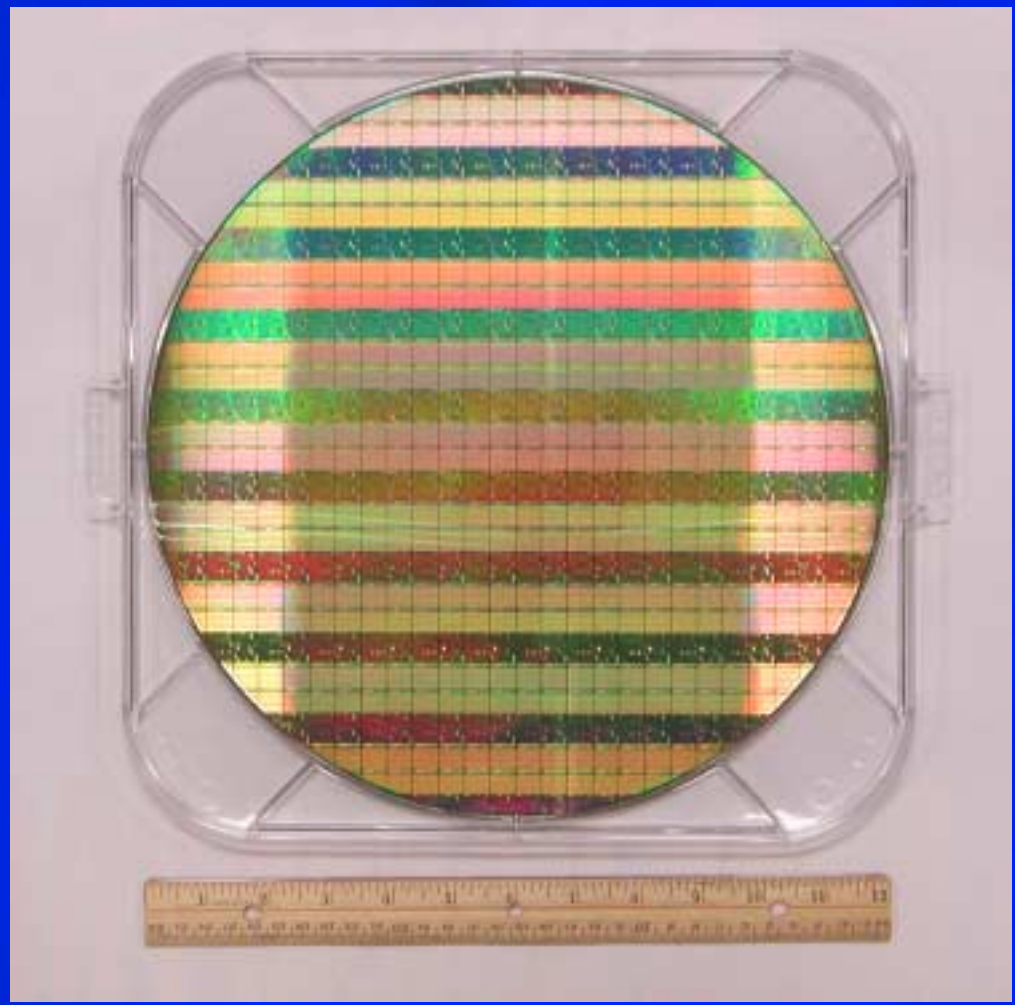
McKinley CPU

Moore's Law Continues



52 Mbit SRAM Chips on 300 mm Wafer

120 billion transistors on one wafer!



Additional Manufacturing Details

- The 90 nm technology is being developed at Intel's 300 mm fab (D1C) in Hillsboro, OR
- 75% of 300 mm process tools used on 0.13 µm process are also used on the 90 nm process
- The 90 nm process will be ramped to high volume in D1C and transferred to other 300 mm manufacturing fabs, starting in 2003
- The lead 90 nm product will be the processor codenamed *Prescott*, (next-generation processor based on NetBurst™ micro-architecture) to be introduced in second half of 2003

90 nm Communication Process

- Intel has developed a feature-rich version of its 90 nm process optimized for communication products
- Shows that Intel is committed to delivering leading edge communication products in high volume
- The 90 nm communication process takes advantage of the performance and manufacturing capabilities of Intel's industry-leading 90 nm logic technology, while adding specialized features for communication products

90 nm Communication Process

Features added for 90 nm communication process:

- High voltage RF analog CMOS transistors
- Precision capacitors and resistors for analog circuits
- High-Q inductors and varactors
- SiGe heterojunction bipolar transistors (HBTs)

Basic features shared with 90 nm logic process:

- High performance, low power digital CMOS transistors using strained silicon technology
- 7 copper interconnect layers + new low-k dielectric
- 1.0 μm^2 SRAM memory cell size
- 300 mm wafers

Added Analog Circuit Elements

High voltage RF CMOS transistors

- Thicker gate oxide allows higher operating voltage which improves signal/noise ratio (dynamic range)

Precision capacitors and resistors

- Two extra masking steps to provide devices with precise control and matching

High-Q inductors

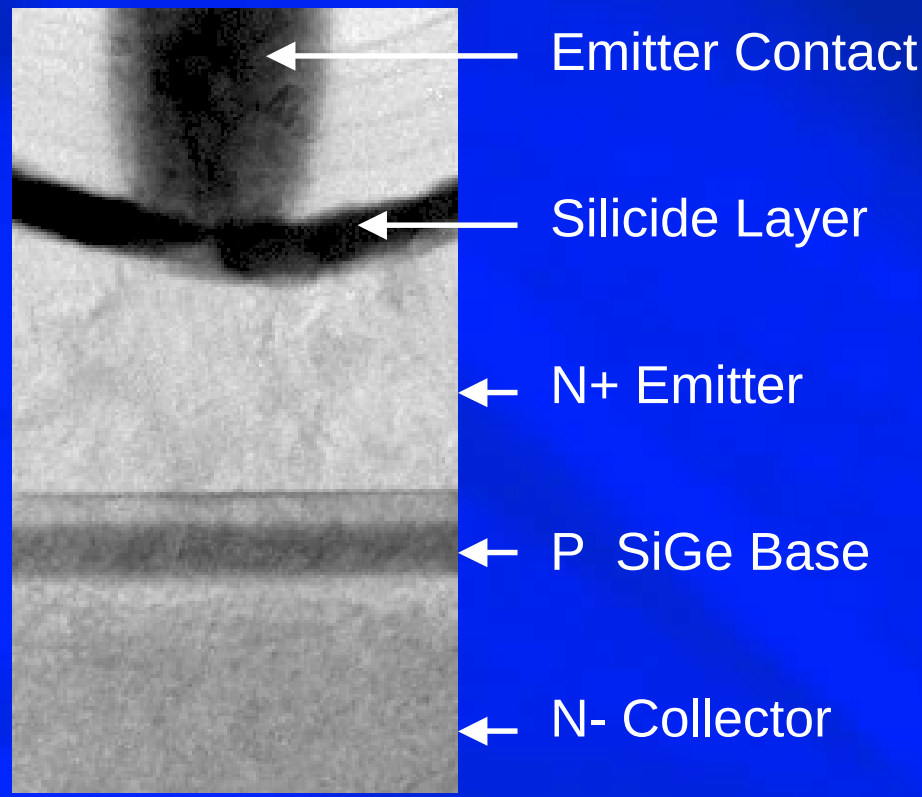
- Thick top copper layer along with high resistance substrate provides high-Q (quality factor) inductor

High-Q varactors

- Voltage-controlled capacitors provided by using standard device elements

SiGe HBT Transistors

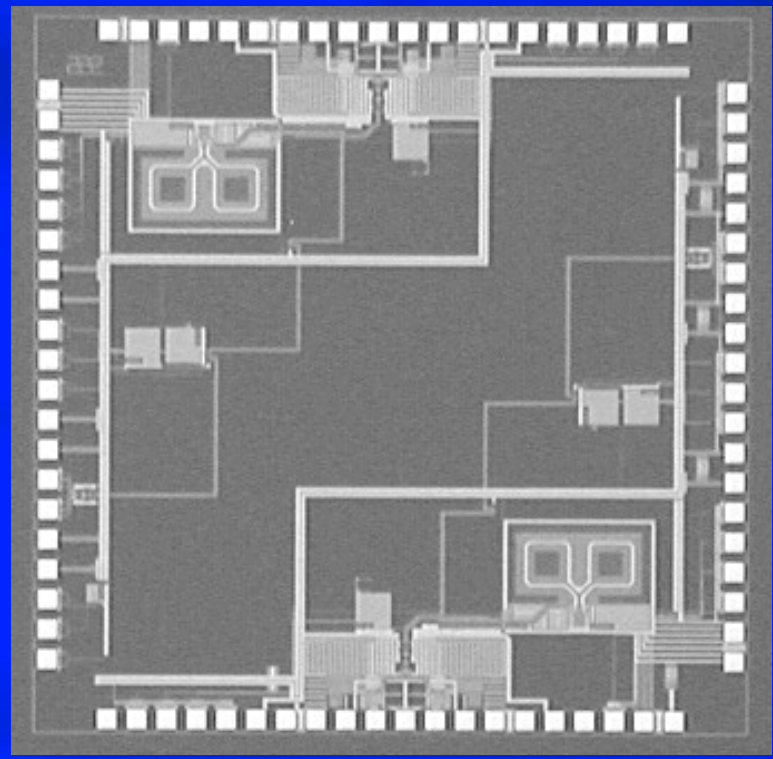
- SiGe HBTs added for high bandwidth communication needs
- SiGe HBTs provide higher frequency, higher voltage swing and lower noise than CMOS transistors
- Added process steps do not impact digital CMOS performance



HBT Cross-section

10 Gb/s SerDes Test Circuits

Application of this process to communication products has been demonstrated on test circuits typically used on 10 Gb/s SerDes products (serializer/deserializer)



Communication Test Circuit

Additional Manufacturing Details

- Both communication and logic versions of the 90 nm process are being developed at Intel's 300 mm fab (D1C) in Hillsboro, OR
- The same 300 mm process tool set is used for both versions, with the exception of the added SiGe deposition tool for HBTs
- Use of the same tool set ensures low cost and ease of manufacturing
- Both versions will be ramped to high volume in D1C on 300 mm wafers starting in 2003

Beyond 90 nm

Process Name	P856	P858	Px60	P1262	P1264	P1266
1st Production	1997	1999	2001	2003	2005	2007
Lithography	0.25µm	0.18µm	0.13µm	90nm	65nm	45nm
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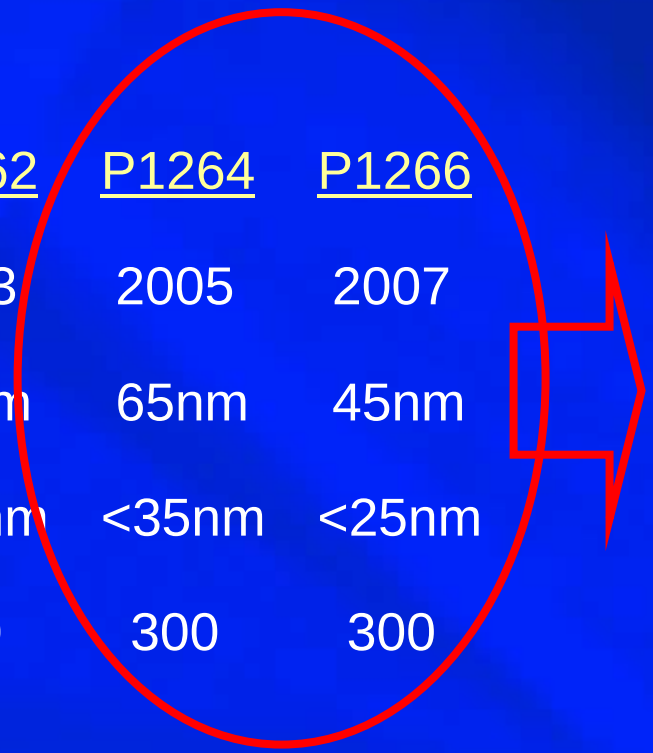


Lithography

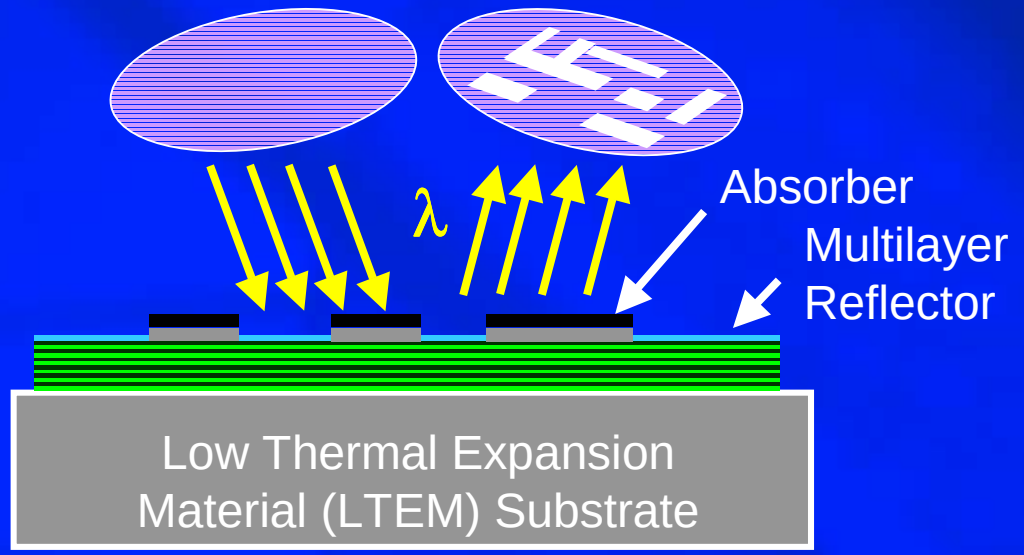
Challenge: Implement cost effective way to print ever-smaller dimensions

One Approach: Shrink wavelength of exposure light

- 248 nm wavelength — manufacturing
- 193 nm wavelength — near-manufacturing
- 157 nm wavelength — development
- 13 nm (EUV) wavelength — research

Extreme Ultraviolet (EUV) Lithography

EUV Prototype in Livermore CA

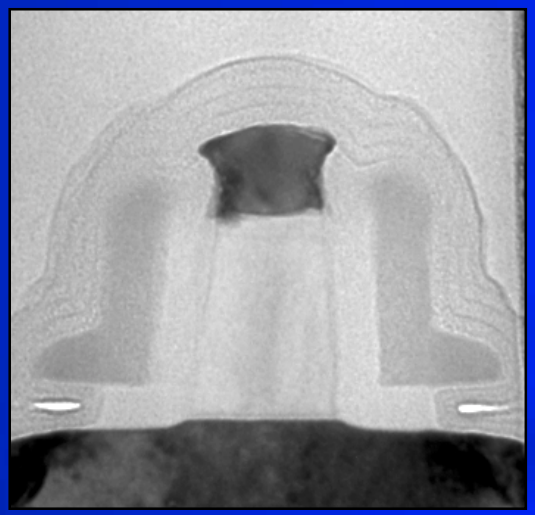


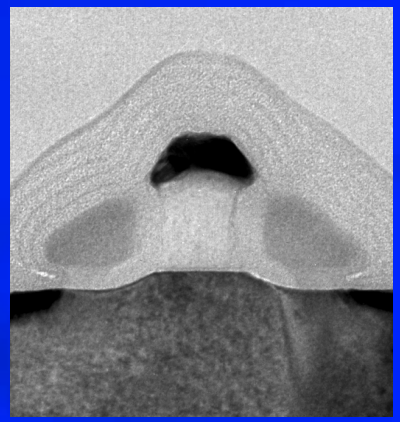
Reflective Mask

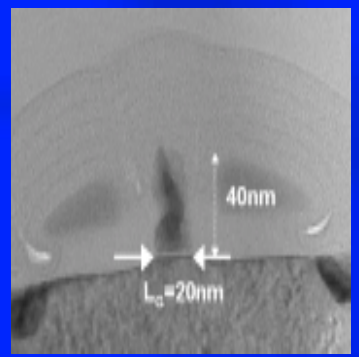
Planar CMOS Transistor Scaling

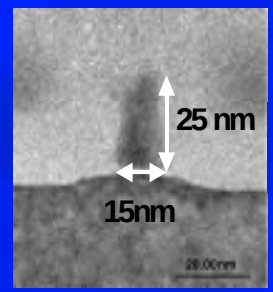
Today

Future





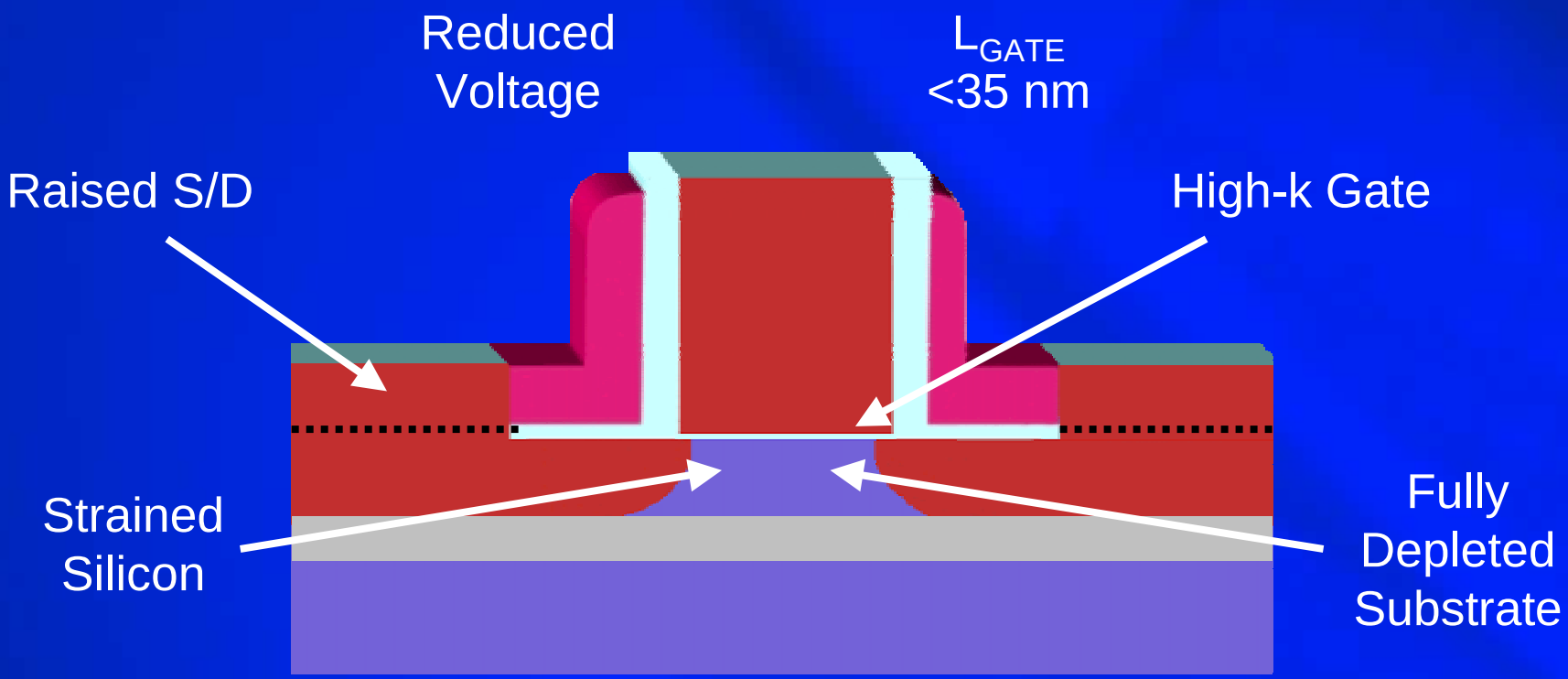




50 nm L_{GATE} 30 nm L_{GATE} 20 nm L_{GATE} 15 nm L_{GATE}

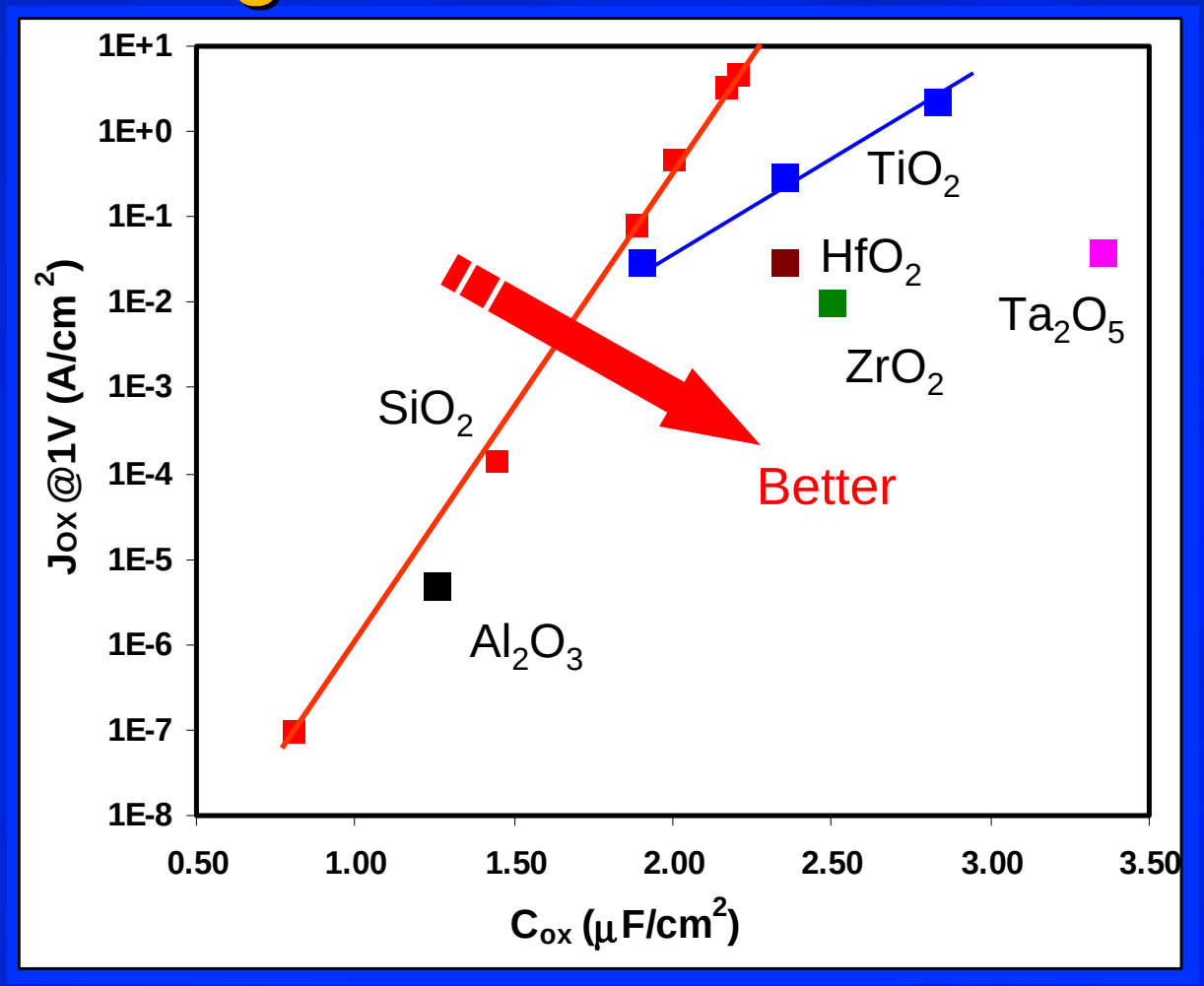
Intel R&D groups exploring aggressive scaling of conventional planar CMOS transistors

Future TeraHertz Transistor



New process options being explored for the future TeraHertz transistor

High-k Gate Dielectric

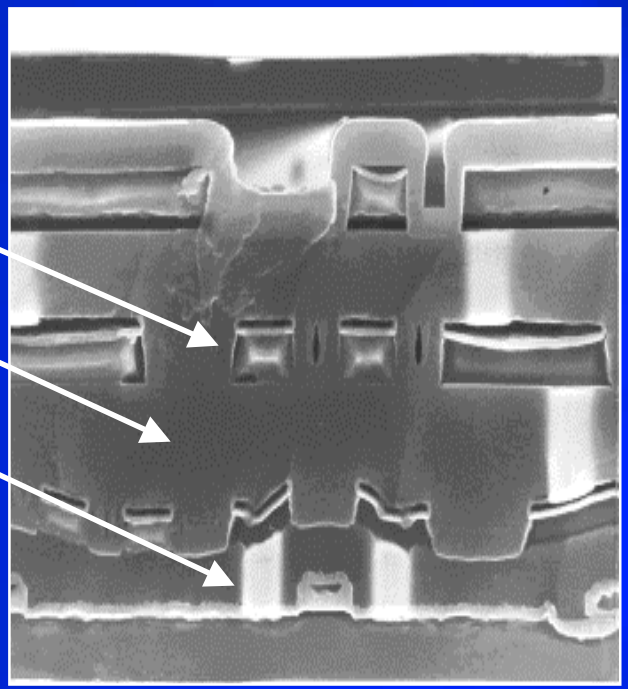


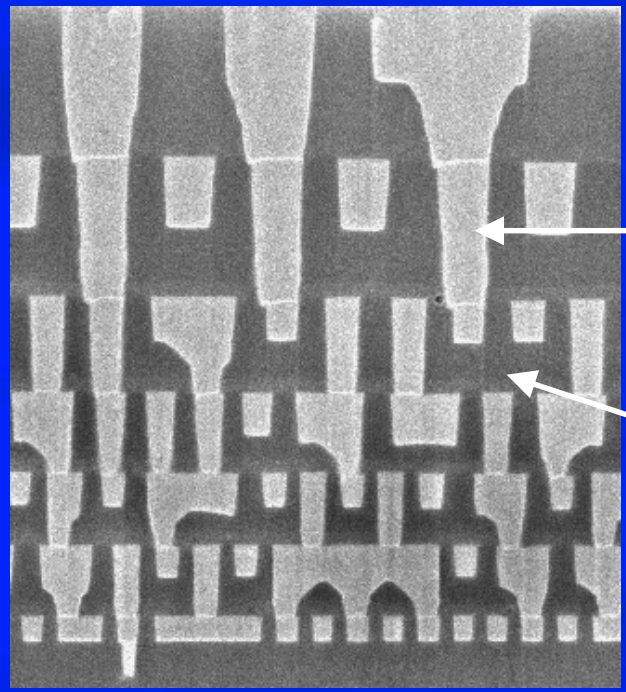
High-k dielectrics provide higher capacitance and reduced leakage

Continued Progress on Interconnects

0.5 µm Interconnects

90 nm Interconnects





3 Layers

7 Layers

Five Generations of Interconnect Progress

Summary

- Intel's 90 nm logic technology incorporates these industry-leading features: high performance strained silicon transistors, 7 copper layers with low-k dielectric, 1.0 μm^2 SRAM cell, and 300 mm wafers
- A feature-rich 90 nm communication process has been developed that includes the main features of the logic process while adding specialized analog device elements and SiGe HBT transistors
- Intel has the world's most advanced 90 nm process and will be first to ship 90 nm products in 2003
- We still have not found a device physics barrier to extending Moore's Law beyond 90 nm

Additional details of Intel's 90 nm technology will be presented at the International Electron Devices Meeting (IEDM) in San Francisco in December 2002

For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon